IN THE CLAIMS:

Claims 5, 6 and 23 have been amended herein. All of the pending claims 1 through 25 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

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Listing of Claims:

1. (previously presented) A method for testing a plurality of semiconductor components, comprising:

forming a plurality of dice on a semiconductor wafer, the plurality of dice each including at least one die contact; and

forming at least one wafer-level redistribution circuit on each of the plurality of dice for interconnection with others of the plurality of dice, the at least one wafer-level redistribution circuit including a redistribution circuit, and a bus conductor traversing each of the plurality of dice for electrically coupling with at least another one of the plurality of dice and at least one conductor for coupling the redistribution circuit to the bus conductor.

2. (previously presented) The method, as recited in claim 1, further comprising forming an outer passivation layer on an exposed face of the semiconductor wafer covering the redistribution circuit and the bus conductor.

3. (previously presented) The method, as recited in claim 2, further comprising probing each of the plurality of dice to determine functional and nonfunctional dice.

4. (original) The method, as recited in claim 3, further comprising storing location information on nonfunctional dice.